The vectored interrupt

By David G. Larsen, Peter R. Rony, and Jonathan A. Titus

THIS MONTH, we continue the discussion of computer interrupts, with emphasis upon vector interrupt hardware and software associated with the 8080A microprocessor chip. The three signals used in vector interrupt circuits include INT (input pin 14 on the 8080A chip), INTE (output pin 16), and INTA, not available on the 8080A chip but derived externally with additional logic.

A positive clock pulse from an interrupting device supplies a logic 1 state at the INT, or *interrupt request,* input that generates an interrupt request, which the CPU recognizes either at the end of the current instruction being executed or while the CPU is in the halt state. The INTE, or *interrupt enable,* output pin indicates the logic state of the interrupt enable flip-flop present within the 8080A chip. This internal flip-flop can be set (enabled) or cleared (disabled) with the aid of 8080A microcomputer instructions:

363	DI	Disable interrupt flip-flop
373	EI	Enable interrupt flip-flop

When cleared, the interrupt enable flip-flop inhibits interrupts from being accepted by the CPU. The flip-flop is automatically cleared when an interrupt is accepted; it is also cleared by the RESET input signal applied at pin 12 of the 8080A chip.

The INTA, or *interrupt acknowledge,* control signal is generated by applying the INTA and DBIN control signals to a two-input NAND gate *(Figure* 1). A logic 1 at DBIN (output pin 17 on the 8080A chip), or *data bus in,* indicates to external devices that the data bus is in the input mode. The INTA control signal is a positive clock pulse that is generated as a status output with the aid of a status latch connected to the 8080A microprocessor chip' ,2; we shall talk about the status latch in a subsequent column. The interesting aspect of the INTA control signal is that it permits you to "jam" an interrupt vector instruction byte directly into the instruction register within the 8080A chip. This can only be done during an interrupt, but nevertheless it is a unique and highly interesting operation that is possible with the 8080A microprocessor.

A simple circuit that demonstrates how a single-byte instruction can be jammed into the instruction register is provided in *Figure 2.* Assuming that the interrupt enable flip-flop has been enabled previously by the instruction, 373, the interrupting device must supply a logic 1 input at INT in order to generate an interrupt request. The

Mr. Larsen, Department of Chemistry, and Dr. Rony, Department of Chemical Engineering, are with the Virginia Polytechnic Institute and State University. Mr. Titus is *President, Tychon, Inc.*

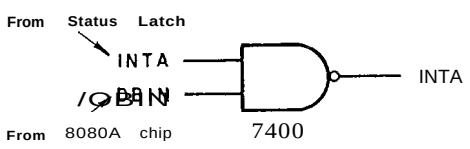

Figure 1 *The INTA control signal is generated from the DBIN and INTA control signals, only one of which is available on the BOBOA chip.*

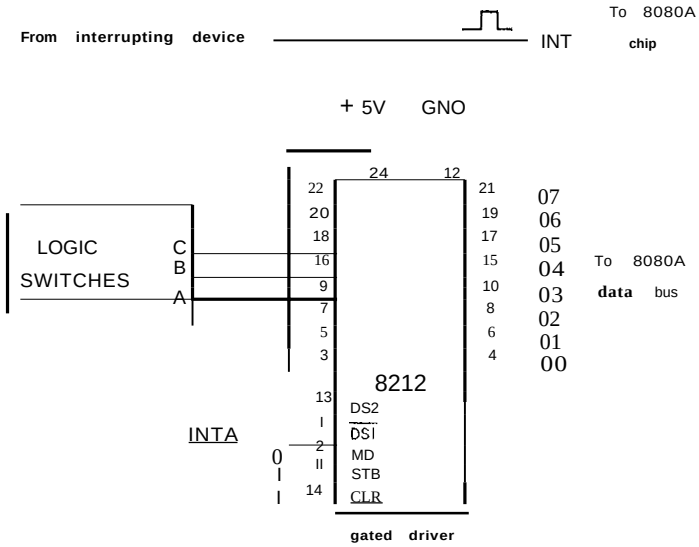

Figure 2 *Interface circuit for the jamming of a single-byte instruction into the instruction register of an 80BOA microprocessor chip.*

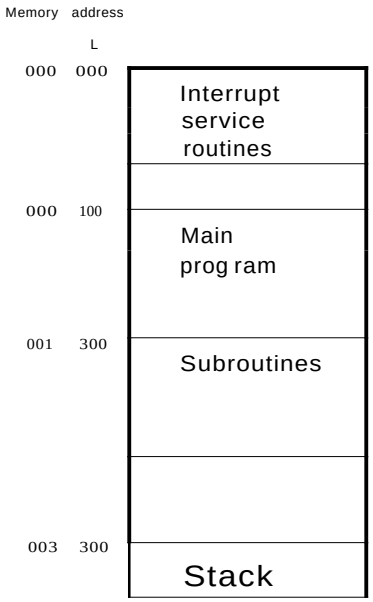

Figure 3 *Possible memory "map" for 8080A microcomputers.*

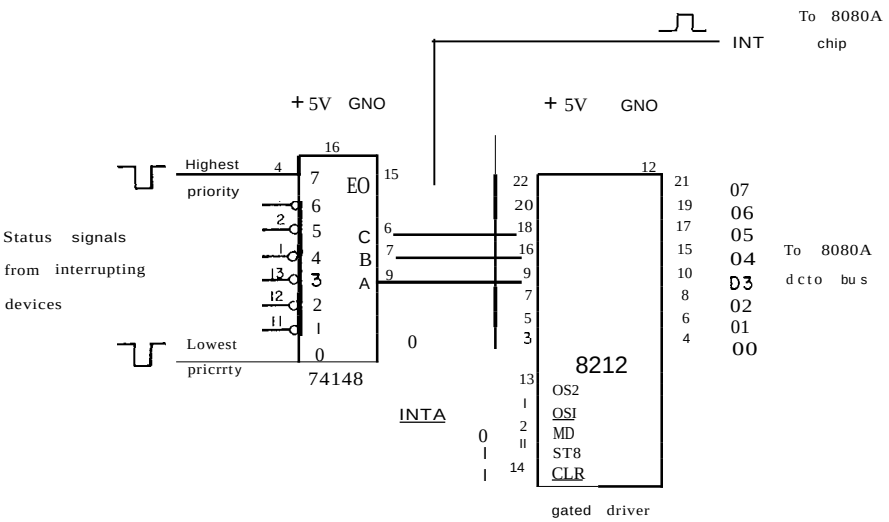

Figure 4 *Priority interrupt encoding scheme for 8080A microcomputers.*

microcomputer finishes the current instruction, and then generates the interrupt acknowledge signal, INTA, which jams the desired vector instruction byte on the data bus and into the instruction register. Although any interruption byte can be jammed into the instruction register during an interrupt, usually the eight instructions listed in *Table* 1 are used to produce a useful result. Thus, the first sixty-four memory locations are reserved for *interrupt service routines* or *pointers,* extremely short programs, often consisting of only a single-jump instruction, that tell the 8080 microcomputer what to do or where to go for a specified interrupt condition. Such routines precede the main program and associated subroutines in memory *(Figure* 3). If interrupts or restart instructions are not used, this portion of memory does not have any special significance.

Figure 4 is probably the simplest priority encoder interrupt circuit that can be used with an 8080 microcomputer. The Intel 8212 chip is used as an 8-bit three-state buffer that inputs the instruction byte into the instruction register. The 74148 8-line-to-3-line priority encoder chip has the truth table shown in *Table 2.*

The purpose of the circuit in Figure 4 is to input the restart instruction, 3Y7, into the microcomputer. Five of the eight inputs to the 8212 chip are tied to a logic 1 state. The remaining three bits supply the encoded vector address of the restart subroutine. By virtue of its truth table, the 74148 priority encoder chip provides eight priority levels. The inputs to this chip should be latched. The chip provides the three-bit binary output that corresponds to the highest valued priority input which is at a logic 0 state. The inverters invert this information to supply the three-bit "Y" component of the restart instruction. If there is a logic 0 at any of the inputs to the 74148 chip, a logic 1 output will be generated at the EO output (pin 15). This output serves as the input to the interrupt request pin, INT, on the 8080A chip. Upon receiving an interrupt request, the microcomputer responds with an interrupt acknowledge output, INTA, that strobes the selected highest priority restart instruction into the instruction register.

References

1. "Intel 8080 Microcomputer Systems User's Manual" (Intel Corporation, Santa Clara, Sept. 1975).
2. RONY, P.R., LARSEN, D.G., and TITUS, J.A., *Bugbook Ill. 8080 Microcomputer Interfacing Experiments* (E & L Instruments, Inc., Derby, 1975).

Table 1

307	RST 0	Call the subroutine that starts at HI = 000 and LO = 000
317	RST 1	Call the subroutine that starts at HI = 000 and LO = 010
327	RST 2	Call the subroutine that starts at HI = 000 and LO = 020
337	RST 3	Call the subroutine that starts at HI = 000 and LO = 030
347	RST 4	Call the subroutine that starts at HI = 000 and LO = 040
357	RST 5	Call the subroutine that starts at HI = 000 and LO = 050
367	RST 6	Call the subroutine that starts at HI = 000 and LO = 060
377	RST 7	Call the subroutine that starts at HI = 000 and LO = 070

Table 2

Inputs"								Outputs			
0	1	2	3	4	5	6	7	C	B	A	EO
X	X	X	X	X	X	X	0	0	0	0	1
X	X	X	X	X	X	0	1	0	0	1	1
X	X	X	X	X	0	1	1	0	1	0	1
X	X	X	X	0	1	1	1	0	1	1	1
X	X	X	0	1	1	1	1	1	0	0	1
X	X	0	1	1	1	1	1	1	0	1	1
X	0	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	0

aThe letter X means that the logic state is irrelevant.