TITUS LABS
P. O. BOX 242
BLACKSBURG, VA. 24060

TECHNICAL REPORT # 67

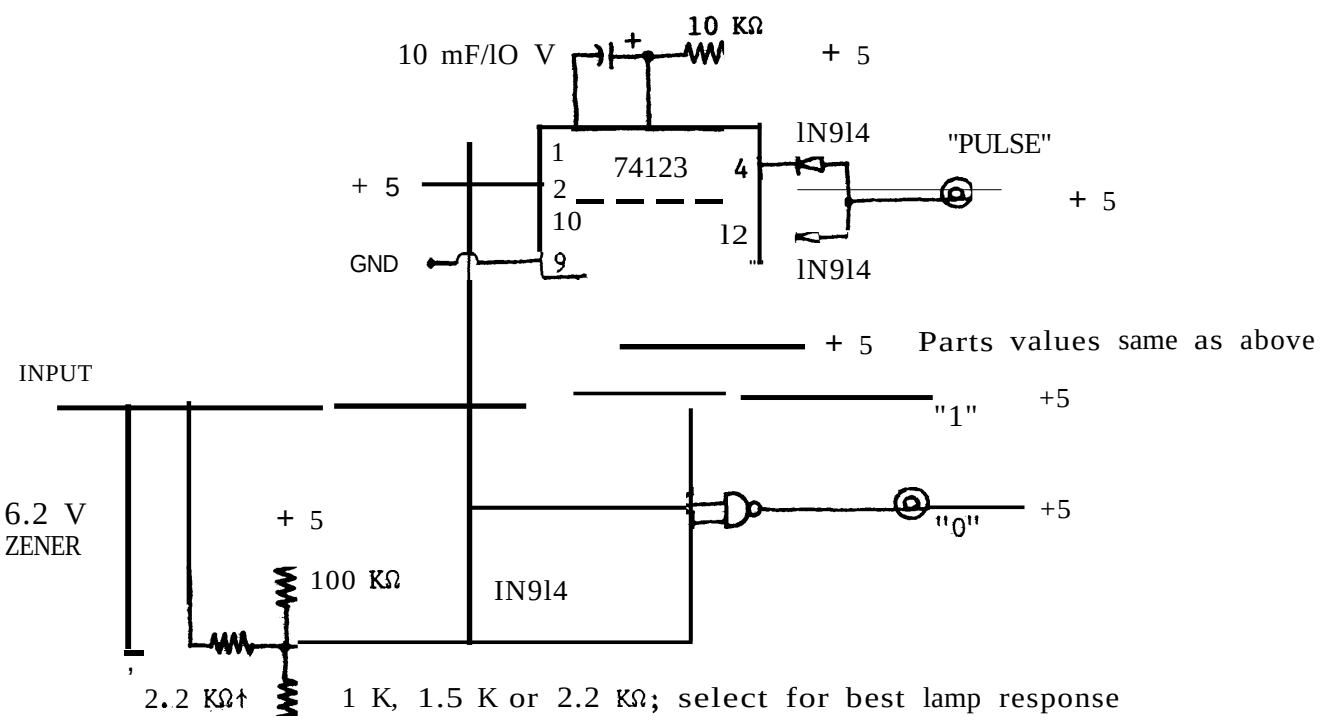
## LOGIC PROBE

This is an extremely simple probe which will detect extremely short pulses, logic levels, and open circuits for standard TTL and DTL circuits.

The first two NAND -gates, A and B, buffer the input signal and then drive the following two NAND gates which then indicate the logic level present by lighting the correct output lamp. The first input NAND gate also drives two monostable circuits (74123), one of which is set to trigger on a positive-going edge and the other is set to trigger on a negative-going edge. The Q outputs of the monostables are ANDed with_two diodes which are then connected to a lamp. When either of the Q outputs go to 0, indicating that the monostable has been triggered, the lamp lights indicating a logic level transition.

The resistor and diode input network will disable the lamp driver NAND gates when no definite input is present at the probe tip. When all the lamps are off it indicates an open circuit at the probe. This makes the probe very useful for detecting open input pins on integrated circuit packages. Open output pins will give a definite logic level•. The red and the clear lamps indicate the logic level present at the input. The flashing of the green lamp will indicate a logic level transition. The monostables are now set for about a 10 to 25 millisecond pulse.

LOGIC PROBE




1 K, 1.5 K or 2.2 KΩ; select for best lamp response

Pin numbers shown for signals to 74123. Use 5 V, 20 mA lamps as indicators. Color for distinguishing the states.

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## LOGIC PULSER PROBE

The Logic Pulser Probe shown in the schematic is an extremely useful tool for anyone testing and designing digital logic circuits. It will provide both a logic 1 and a logic 0 pulse to DTL and TTL type circuits from a normally high impedance state. It is no longer necessary to determine what type of a pulse is needed at a circuit node since the probe will provide a pulse of the opposite logic level. Most probes do not have this feature.

The bounceless switch configuration triggers both of the monostables (74123), but the period of monostable A is twice as long as that of monostable B. A enables the NAND gate and B then strobes each, which then turn on the output transistors in sequence. This causes the probe to go from the normal high impedance or off state to a logic 1 followed by a logic 0 and finally a return to the off state. The off state does not affect the logic circuits under test.

Pulse widths are easily changed by changing the values of the resistor-capacitor network for each monostable. It is best to keep the pulses short and the period of A should be twice that of B to give equal times to both logic level pulses. The 33 ohm resistor may be added for current limiting if needed and the complete circuit may be constructed to fit into a small pocket-sized flashlight case.

LOGIC PULSER PROBE