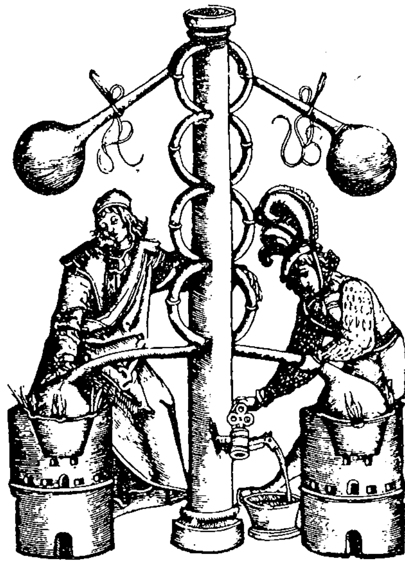

Microcomputer interfacing

Interfacing a lO-bit DAC

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IN THIS COLUMN we shall discuss how to interface an Analog Devices AD7522 monolithic CMOS lO-bit multiplying digital-to-analog converter (DAC), a 28-pin chip which is a recent example of a new generation of inexpensive DACs that can be interfaced directly to 8-bit microcomputers.

A *digital-to-analog converter* is an electronic device that converts digital signals into analog signals. A typical converter consists of an arrangement of weighted resistors, each controlled by a single bit of input data that develops varying output analog voltages or currents in accordance with the digital input code.' A DAC is used to provide a small analog error signal from a microcomputer that is used in a feedback control circuit; to convert a sequence of bytes in memory into analog-vs-time data and thus simulate the output from an analog instrument such as a gas chromatograph or uv-visible spectrophotometer; to provide analog data for the two channels of an X-Y recorder; or, in general, to operate any device that requires an analog voltage or current and is interfaced to a digital device, such as a microcomputer.

For a general discussion of the principles of analogidigital conversion, we refer you to the excellent Analog Devices conversion handbook' or to the series of small pamphlets distributed by National Semiconductor Corporation.' Important concepts associated with DACs include resolution, accuracy, scale error, ,gain error, offset error, linearity, differential linearity, monotonicity, settling time, slew rate, overshoot and glitches, temperature coefficient, supply rejection, conversion rate, and output drive capability.[2] Definitions for a few such terms are summarized in *Tablef.*

To help you understand how to in-

Table 1

Some important concepts associated with digital-to·analog converters

Resolution	The smallest standard incremental change in output voltage of a DAC. A converter with *n* input bits can resolve one part in 2^n.
Accuracy	Describes the worst-case deviation of the DAC output voltage from a straight line drawn between zero and full scale; it includes all errors.
Settling time	The elapsed time after a code transition for a DAC output to reach a final value within specified limits.
Conversion rate	The speed at which a DAC can make repetitive data conversions.
Nonlinearity	Error contributed by a deviation of the DAC transfer function from a best straight-line function. Normally expressed as a percentage of full-scale range.
Monolithic chip	An integrated circuit chip in which both active and passive elements are formed simultaneously in a single small silicon wafer via the use of diffusion and epitaxial processes. Metallic strip's are evaporated onto the oxidized surface of the silicon to interconnect the elements.
Multiplying DAC	A digital-to-analog converter in which the output analog signal is the product of the number represented by the digital input code and the input analog reference voltage, which may vary from full scale to zero, and in some cases, even to negative values.
CMOS	Complementary metal-oxide-semiconductor technology. A key advantage is extremely low power dissipation. Used in battery-operated systems. Also has good noise immunity.

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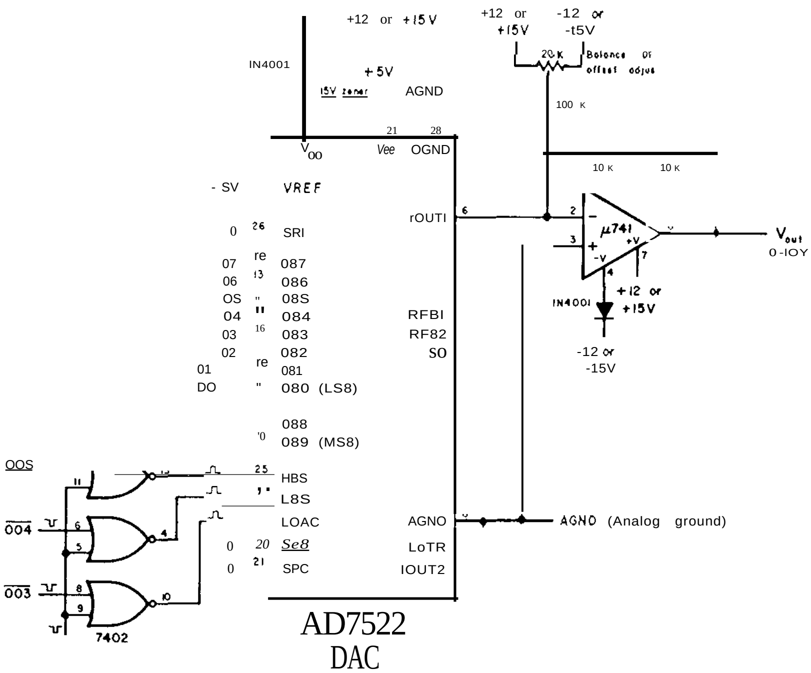
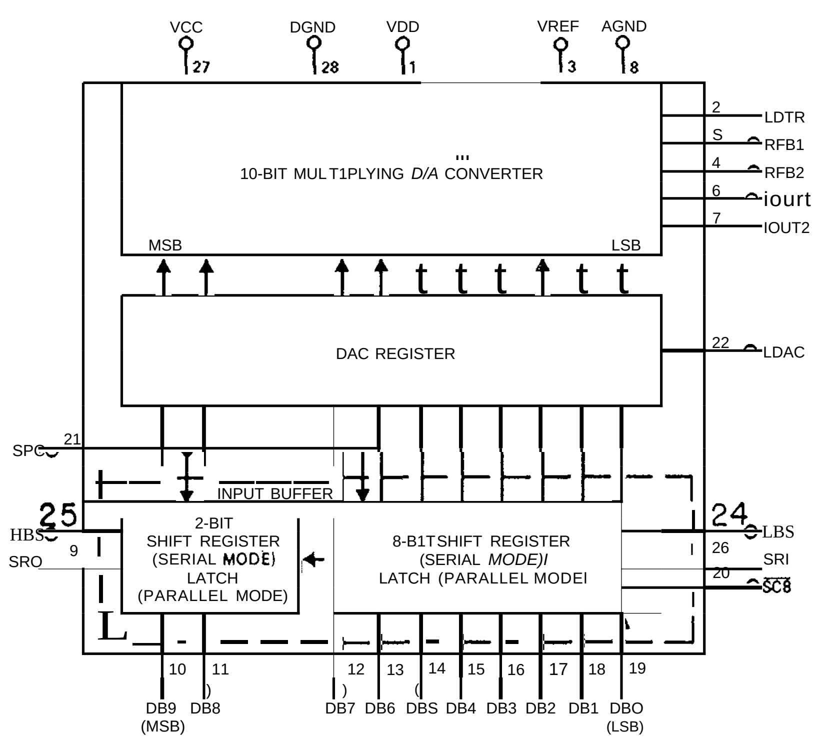


Figure 1 *Interface circuit between an 8080A-based microcomputer and an AD7522 digital-to-analog converter chip.*

terface the AD7522 DAC to an 8-bit microcomputer, both an interface circuit to an 8080A-based microcomputer *(Figure* 1) and a functional diagram of the DAC *(Figure* 2*) are provided. An important feature of this specific DAC is the fact that it is *double buffered;* this means that there exist within the device two independent lO-bit registers, the DAC register, and the two-bit and eight-bit shift registers noted as the input buffer (Figure 2). A DAC is an output' device for a microcomputer, and thus data are strobed from the microcomputer data bus into the internal registers or latches of the DAC. In Figure I, we show the connections to the 8-bit bidirectional data bus, DO through D7; the 8080A control signals OUT or MEMW, which are used with accumulator I/O or memory I/O data transfers'; and the channel select outputs 003 through 005 that are generated by a decoder tied to the microcomputer address bus.'

Figure 2 *Functional diagram of the AD7522 chip.*



Since the AD7522 is a lO-bit DAC, it is not possible to load all ten bits simultaneously into the input buffer (Figure 2) of the DAC from an 8-bit microcomputer. The sequence that actually occurs can be summarized as follows: I) The DAC input bits DBO through DB7 are first strobed into the 8-bit shift register/latch in parallel using a positive *device select pulse'* applied at input pin 24, LBS or low byte strobe; 2) The most significant two bits, DB8 and DB9, are then strobed into the 2-bit shift register/latch via the use of a device select pulse applied at pin 25, HBS or high byte strobe; 3) Finally, a device select pulse applied at pin 22, LDAC or load DAC, transfers the ten bits of input data, DBO through DB9,' into the second buffer within the DAC chip, the DAC register, from which the D/A conversion is performed. The output current apears at 10UTl and IOUT2 and is converted into a voltage with the aid of a µ741 operational amplifier (Figure I). The two most significant bits are loaded

• Courtesy of Analog Devices, Inc.

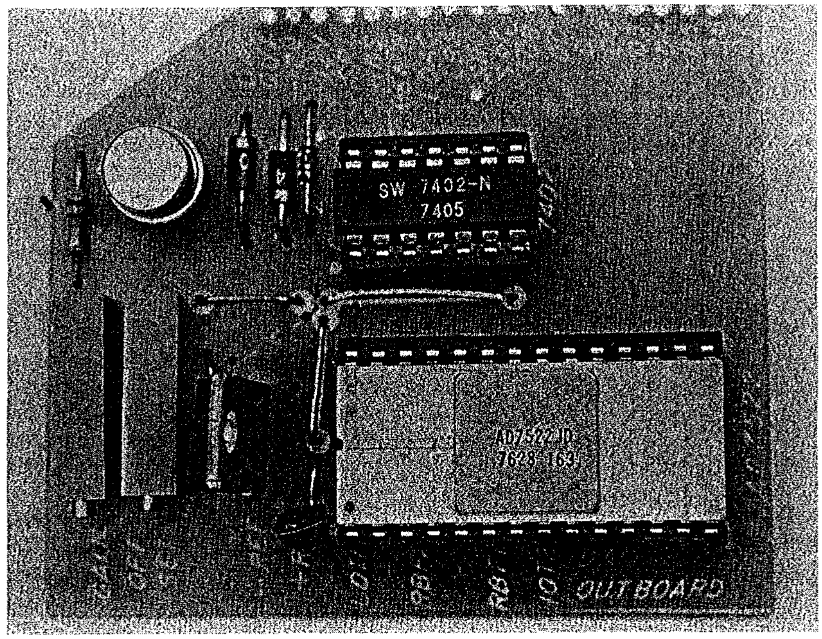


Figure 3 *Photograph of the DAG Outboera» that contains the circuit shown in Figure 1.*

from the eight-bit microcomputer bus using any two bits. Generally bits DO and Dl are chosen since it makes data fomatting easy. Thus, the ten bits are transferred as eight bits DO to D7 and as two additional bits, DO and Dl.

A simple program that exercises the DAC over its full operating range is provided in *Table* 2. The program generates a slow linear ramp as the analog voltage output from the AD7522 DAC. This can be observed on a YOM, digital multimeter, or oscilloscope. The ramp output is subdivided into 1024 small steps, each step being approximately 5 mv in magnitude. The total time required to change from 0.0 to + 5.12 v is 10.24 sec. The SHLD <B2> B3> instruction outputs two data bytes in succession from register pair H into the input buffer registers of the DAC. The contents of register L are input into the 8-bit shift register/latch and the least significant two bits in register Hare input into the 2-bit shift register/latch (Figure 2). *Note that the address* is *automatically incremented and a second MEMW control pulse generated by the 8080A when it executes a SHLD instruction.* The STA < B2 > < B3 > instruction provides only a strobe pulse at the LDAC input to the DAC; no data transfer occurs between the accumulator and the DAC.

Additional small monolithic and hybrid DAC systems are available from other manufacturers. The Analog Devices converter was chosen here because of the on-the-chip latches and double buffering registers. The use of a reference potential is common to many DAC modules. Perhaps in the future it, too, will be included in the module.

We refer the reader to the specification sheets for additional information concerning the use of the Analog Devices AD7522 DAC. Since the input buffer is a shift register, it

Table 2

Memory 110 program to generate a slow linear ramp-

LO address byte	Instruction byte	Mnemonic	Comments
START			
000	042	SHLD	Strobe ten bits of digital data into the AD7522 DAG shift registers. The ten input data bits are contained in register pair H. The address select code for the LBS input is HI = 200 and LO = 004; the address select code for the HBS input is HI = 200 and LO = 005.
001	004	004	
002	200	200	
003	062	STA	Strobe ten bits of digital data from the input buffer into the DAC register within the AD7522 DAC. The address select code for the LDAC input is HI = 200 and LO = 003.
004	003	003	
005	200	200	
006	043	INXH	Increment register pair H
007	315	CALL[b]	Call10-msec tirne-delay routine, DELAY
010	277	277	LO address byte of DELAY
011	000	000	HI address byte of DELAY
012	303	JMP	Unconditional jump to START, where the input of new data into the DAC occurs
013	000	000	LO address byte of START
014	003	003	HI address byte of START

a Execution starts at HI = 003 and LO = 000.

b On the 8080-based microcomputer that we use in our courses, a 10-msec time-delay subroutine is located in EPROM starting at HI = 000 and LO = 277. Such a routine can be located anywhere in memory.

is possible to load the DAC serially. Less expensive 8-bit versions of the DAC are available. The output from the DAC can be either unipolar or bipolar. For use in our short courses in microcomputer interfacing, we have developed a DAC Outboard" that contains everything in Figure 1, including the 5-v reference source *(Figure* 3). If you send a self-addressed stamped envelope, we would be delighted to send you a copy of the PC layout for the board.

References

1. *Analog-Digital Conversion Handbook* (Analog Devices, Inc., Norwood, Mass.).
2. Publication AN-I 56, "Specifying A/D and D/A converters," is particularly useful. Also available is publication AN-159, "Data acquisition system interface to computers" and data sheets on the DA 1200/ 1201/1202/1203 monolithic DACs. (National Semiconductor Corp., Semiconductor Div., Santa Clara, Calif.).
3. RONY, P.R., TITUS, *I.A.*, and LARSEN, D.G., "Microcomputer interfacing: Accumulator I/O vs memory I/O," *Amer. Lab.* 8 (2), 119 (1916).
4. *Bugbook V, Module Six. Introductory Experiments in Digital Electronics, 80SOA Microcomputer Programming, and 8080A Microcomputer Interfacing* (E & L Instruments, Inc., Derby, Conn., 1976).
5. LARSEN, D.G., RONY, P.R., and TITUS, *I.A.*, "Microcomputer interfacing: Generating input/output device select pulses," *Amer. Lab.* 8 (I), 77 (1976).