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Input/Output: A Closer Look

In Chapter 5 we described how the 6800 has to effect all data transfers between the microprocessor system and the outside world by means of memory-mapped I/O ports.* While a simple latch may serve as an adequate output port for an LED display, or a tri-state buffer may be perfect for sensing the position of a switch, the general-purpose microprocessor system needs a more sophisticted form of I/O to deal with the wide range of devices to which it may be connected.

In order to free the CPU from the mundane tasks associated with input or output operations, the microprocessor manufacturers have provided the engineer with a broad spectrum of interface devices. These I/O devices often have circuit complexities which rival those of the CPU itself. If the cost of LSI interface chips is to be kept down, they must be manufactured in large quantities and hence any given chip must be versatile enough for a wide range of applications. This versatility is made possible by making a multi-function I/O device and then allowing the particular function required to be selectable under software control. For example, a typical parallel port has eight lines which can be defined as inputs or outputs (or any combination of either) simply by loading the appropriate control code into one of the peripheral's registers.

The currently available input/output peripherals may be loosely grouped into three types:

(1) *Serial ports* This group includes those peripherals which communicate with each other, or with other external devices, by means of a single data link (or two links if bidirectional data tranfers are required). Such devices are commonly employed to interface the CPU with a VDT or a Teletype, or with another microprocessor system which is situated remotely. Serial ports are able to take a byte of data (or part of a byte) and transmit it serially, bit by bit.

* An exception to this rule is input/output by means of DMA, where data is transferred between the system memory and peripherals without the intervention of the CPU.