MARK-8 BUS SIGNAL DESCRIPTION

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INTER-BOARD WIRE NO.	FUNCTION	SOURCE BOARDS	DESTINATION BOARDS	SYMBOL(S)
1	OUT PORT MSB R BIT	MA	CPU	A13,R2
2	not used			
3	COMMOM GROUND		ALL	GND GROUND
4	STATE CONTROL SIGNAL	CPU	DI	SO SLO
5	STATE CONTROL SIGNAL	CPU	DI	S1 SL1
6	+5 VOLT POWER		ALL	+5
7	-9 VOLT POWER		MA CPU	-9
8	CPU READY LEVEL	MA	CPU	RDY,READY
9	MEMORY ADDRESS &	MA	CPU	D0
10				D1
11				D2
12				D3
13				D4
14	INPUT BUS LINES *	DI	MM,OL	D5
15				D6
16				D7
17	I/O OUTPUT SIGNAL **	CPU	***	OUT OUTPUT
18	OUTPUT BUS LINES	CPU	MA,MM	D7
19				D6
20				D5
21				D4
22				D3
23				D2
24				D1
25				D0
26	MEMORY READ/WRITE SIGNAL	CPU	MM	R/W
27	I/O INPUT SIGNAL	CPU	DI	IN
28	170 OUTPUT SIGNAL	CPU	OL	OUT
29	CYCLE CONTROL SIGNAL	MA	CPU	CC1
30	CYCLE CONTROL SIGNAL	MA	CPU	CC0
31	CPU LAL SIGNAL	CPU	MA	LAL
32	CPU LAH SIGNAL	CPU	MA	LAH
33	OUT PORT LSB R BIT	MA	CPU	A12 R1
34	I/O DATA ENABLE SIGNAL	CPU	DI,OL	DEN
35	170 INTERRUPT SIGNAL	MA	CPU	INT
36	KEYBOARD INTERRUPT	MA	CPU	EX INT
37	CPU WAIT FLAG ****	CPU	N/C	FLAG
38	HIGH MEMORY. ADD. BIT	MA	MM	A
39	DITTO & I/O PORT BIT	MA	MM DI OL	B
40	DITTO & DITTO	MA	MM DI OL	C
41	DITTO & DITTO *****	MA	MM DI,OL	D

* Memory address lines and input bus lines are not common.

** Titus expansion signal for additonal output ports (note: it bypasses the RR≠00 condition,).

*** for Titus' port expansion logic.

**** apparantely for slow memories

***** Wires 39-41 serve a double duty as shown above.

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